PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: ITSUO HIDAKA	
Appl. No.: 09/525,802	Art Unit: 2815
Filed: March 15, 2000	Examiner: CRUZ, L.
For: SEMICONDUCTOR DEVICE	Atty Docket: AKM-00301

CERTIFICATE OF MAILING

I hereby certify that the foregoing document is being deposited with the United States Postal Service as first class mail, postage prepaid, "Post Office to Addressee", in an envelope addressed to: Commissioner of Patents, Washington, DC 20231 on September 12, 2000.

Raymond Bartight

AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is being provided in response to the Office Action dated June 21, 2000, for the above-captioned U.S. patent application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required for consideration of this paper (including fees for net addition of claims) are authorized to be charged in two originally-executed copies of an Amendment Transmittal Letter filed herewith.

Kindly enter the following amendments:

IN THE CLAIMS:

Please amend Claims 1 - 18 as follows:

1. (Amended) A semiconductor device having multiple wiring, layers, comprising:

a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;

a signal line which is formed in [a] one of said wiring [layer] layers, and to which a signal voltage is applied;

two adjacent lines which are [so] disposed adjacent to said signal line so as not to be connected thereto, and which are formed in a same one of said plurality of wiring [layer] layers where said signal line is formed;

two intersection lines which are respectively formed in different ones of said plurality of wiring layers, each of said intersection lines being [present] separated from said signal line via [an] one of said plurality of insulating [layer] layers above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines.

2. (Amended) The semiconductor device according to claim 1, wherein said two adjacent lines, which are formed in said same one of said plurality of wiring layers where said signal line is formed, are formed substantially in parallel to said signal line.

3. (Amended) The semiconductor device according to claim 1, wherein electric potentials of said two adjacent lines formed in the same wiring layer as said signal line, said two intersection lines and said entire-line-area through-holes are [retained] at a predetermined electric potential value.

4. (Amended) The semiconductor device according, to claim 1, wherein [the] electric potentials of said two adjacent lines formed in the same wiring layer as said signal line, said two intersection lines and said entire-line-area [through-hole] through-holes have a same phase as a phase of an electric potential of said signal line.

5. (Amended) A semiconductor device having multiple wiring layers, comprising:

a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;

a plurality of signal lines which are formed not to intersect each other in an identical one of said plurality of wiring [layer] layers, and to which signal voltages having a same phase are applied;

two adjacent lines which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the identical one of said plurality of wiring [layer] layers where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being [present] separated from said signal lines via selected ones of said plurality of insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines.

6. (Amended) The semiconductor device according to claim 5, wherein electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes are [retained] at a predetermined electric potential value.

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5 7. (Amended) The semiconductor device according to claim [6] 3, wherein [the] electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes have a same phase as a phase of an electric potential of said signal lines.

8. (Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;

a plurality of signal lines which are formed not to intersect each other in an identical one of said plurality of wiring [layer] layers, and to which signal voltage having different phases are applied;

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto, and which are formed in the same one of said plurality of wiring [layer] layers where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the same one of said plurality of wiring [layer] layers where said plurality of signal lines are formed, between said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines.

9. (Amended) The semiconductor device according to claim [7] 8, wherein electric potentials of said first and second adjacent lines, said two intersection lines and said entire-line-area through-holes are [retained] at a predetermined electric potential value.

10. (Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;

a plurality of signal lines which are formed substantially in parallel to each other in different ones of said plurality of wiring layers, and to which signals having a same phase are respectively applied;

a plurality of adjacent lines, each pair of which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto in the wiring layers where said plurality of signal lines are formed;

two intersection lines, each of which is formed in a layer under a lowermost wiring layer where said plurality of signal lines are formed or in a layer above an uppermost wiring layer where said plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by said plurality of adjacent lines formed on the both extreme sides of said plurality of signal lines;

a plurality of first entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines and said two intersection lines, along entire areas of said adjacent lines, and which electrically connect said adjacent lines with said two intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines, along the entire areas of said adjacent lines, and which electrically connects said adjacent lines with each other.

9 11. (Amended) The semiconductor device according to claim 8 ~~10~~, wherein electric potentials of said adjacent lines, said two intersection lines and said one or more first and second entire-line-area through-holes are retained at a predetermined electric potential value.

10 12. (Amended) The semiconductor device according to claim [11] 8 ~~10~~, wherein [the] electric potentials of said adjacent lines, said two intersection lines and said one or more first and second entire-line-area through-holes have a same phase as a phase of an electric potential of said signal lines.

13. (Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers;

a plurality of signal lines which are formed in different selected ones of said plurality of wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in a lowermost or uppermost wiring layer[,] of the wiring layers where said plurality of signal lines are formed, respectively adjacent onto both sides of a selected one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of said signal lines, or in a wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines;

a second intersection line which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection [line] lines.

~~14.~~ (Amended) The semiconductor device according to claim ~~13~~, wherein signal voltages which are out of phase with each other are respectively applied to different ones of said plurality of signal lines.

15. (Amended) The semiconductor device according to claim 14, wherein electric potentials of said first and second adjacent lines, said first and second intersection lines and said first and second entire-line-area through-holes have a same phase as an electric potential of said signal lines.

16. (Amended) The semiconductor device according to claim 13, wherein said signal lines formed in different wiring layers which are adjacent to each other intersect each other.

17. (Amended) A semiconductor device having a structure in which a selected one signal line of a plurality of signal lines, to which a selected signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, whose electric potentials are set at a predetermined value.

18. (Amended) A semiconductor device having a structure in which a selected one signal line of a plurality of signal lines, to which a selected signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has a same phase as a phase of said signal line is applied.

REMARKS

This paper is being provided in response to the June 21, 2000 Office Action for the above-referenced application. In this response, Applicant has amended Claims 1 - 18 in order to more particularly point out and distinctly claim that which Applicant deems to be the invention. Applicant respectfully submits that the amendments to the claims are

all supported by the originally filed application. The objection to the drawings is addressed by the request for drawing changes attached to this response in which figures 8 and 9 have had the legend "Prior Art" added.

The rejection of Claims 1 - 4 under 35 U.S.C. §102(b) as being anticipated by Landis (U.S. Patent No. 4,673,904, hereinafter referred to as "Landis") is hereby traversed and reconsideration thereof is respectfully requested. Applicants respectfully submit that Claims 1 - 4, as amended herein, are patentably distinct over the cited reference.

Independent Claim 1, as amended herein, recites a semiconductor device having multiple wiring layers with individual semiconductor devices on a semiconductor substrate having insulating layers between patterned conductor wiring layers. A signal line which is formed in one of the wiring layers, and to which a signal voltage is applied, has two adjacent lines which are adjacent to the signal line but not connected, and which are formed in the same wiring layer as the signal line. There are two intersection lines which are formed in different wiring layers, and each intersection line is separated from the signal line via one of the insulating layers, either above or under the signal wire, and are formed along a surface area corresponding to an area which is enclosed by the two adjacent lines. A plurality of entire-line-area through-holes penetrate through the insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and thus electrically connect the two adjacent lines and the two intersection lines.

Claim 2, as amended herein, recites a semiconductor device where the two adjacent lines, which are formed in the same wiring layer as the signal line, are formed substantially in parallel to the signal line.

Claim 3, as amended herein, recites a semiconductor device where the electric potentials of the two adjacent lines, which are formed in the same wiring layer as the signal line, and the two intersection lines, and the entire-line-area through-holes are at a predetermined value.

Claim 4, as amended herein, recites a semiconductor device with the electric potentials of the two adjacent lines, the two intersection lines and the entire-line-area through-holes, have the same phase as the phase of the signal line.

The cited art of Landis relates to a support board interconnecting various individual electronic components with conductors embedded in the substrate. Each of the conductors has shielding to permit high frequency signals between the individual components without cross coupling interference. The board 20 of figures 2 and 3 has a metallic base (typically copper) and a layer of dielectric material 24 (typically a low dielectric constant material such as polyimide plastic) into which a plurality of conductors are embedded. Depending on the degree of electrical isolation that each of the conductors requires, the shield may be a tube, a "U" or an "I" structure. These shields are formed on the copper base of the board so that they are electrically connected to the ground plane. For terminating purposes the two extreme portions of each conductor have

a vertical section 50 which ends in a square pad flush with the top surface 54 of the board, which then are wirebonded to the pads of the IC's 56 and 58.

Applicant respectfully submits that the cited reference does not contain the recited feature of "...*a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers* ...", as set forth in Applicant's independent claim 1, as amended herein. Rather, the cited reference discloses a printed circuit board made of plastic and having a copper base. Further, the cited reference does not disclose an IC having interconnections between various portions of the IC, but rather a device that is wirebonded to discrete IC mounted upon the PCB. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 1. Dependent claims 2 - 4 depend from independent Claim 1, and contain further patentable limitations, and thus can not be anticipated by the Landis reference. Specifically, the cited reference does not disclose the "electric potentials" of the shield portions "have a same phase as a phase of an electric potential of said signal line", as recited in dependent claim 4.

Accordingly, Applicant respectfully submits that independent Claim 1, as amended herein, and thus dependent Claims 2 - 4, which depend from Claim 1, are patentably distinct over the cited Landis reference, and respectfully requests that this rejection be withdrawn.

The rejection of Claims 5 - 18 under 35 U.S.C. §102(b) as being anticipated by Schreiber et al (U.S. Patent No. 4,845,311, hereinafter referred to as "Schreiber") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 5 - 18, as amended herein, are patentably distinct over the cited reference, for the reasons set forth below.

Independent Claim 5, as amended herein, recites a semiconductor device having multiple wiring layers with a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers. There is a plurality of signal lines which are formed not to intersect each other in an identical wiring layer, and to which signal voltages having the same phase are applied. Two adjacent lines are so formed adjacent onto both sides of the signal lines, but are not connected thereto, and are formed in the same wiring layer as the signal lines are formed. Two intersection lines are formed in a wiring layer and are separated from the signal lines via insulating layers either above or under the wiring layer where the signal lines and two adjacent lines are formed. The intersection lines are formed along a surface area corresponding to an area enclosed by the two adjacent lines. A plurality of entire-line-area through-holes penetrate through the insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and thus electrically connect the two adjacent lines with the two intersection lines, forming the tubular box around the signal line.

Claim 6, as amended herein, recites a semiconductor device where the electric potentials of the two adjacent lines, the two intersection lines and the entire-line-area through-holes are at a predetermined electric potential value.

Claim 7, as amended herein, recites a semiconductor device where the electric potentials of the two adjacent lines, the two intersection lines and the entire-line-area through-holes have the same phase as the signal lines.

Independent Claim 8, as amended herein, recites a semiconductor device having multiple wiring layers, having a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers. A plurality of signal lines are formed not to intersect each other in a wiring layer, and signal voltage having different phases are applied. Two first adjacent lines are formed adjacent respectively onto an outer two of the signal lines, but are not connected thereto, and which are formed in the wiring layer as the signal lines are formed. At least one second adjacent line is formed in the same wiring layer as the signal lines are formed, and are between the signal lines but not connected to the signal lines. There are two intersection lines, each of which is formed in a wiring layer, and separated via an insulating layer, either above or under the wiring layer where the signal lines and the first adjacent lines are formed. Each of which is arranged along a surface area corresponding to an area enclosed by the two first adjacent lines. The entire-line-area through-holes penetrate through the insulating layers formed between the first and second adjacent lines and the two intersection lines along

entire areas of the first and second adjacent lines. This electrically connects the first and second adjacent lines with the two intersection lines.

Claim 9, as amended herein, recites a semiconductor device where the electric potentials of the first and second adjacent lines, the two intersection lines and the entire-line-area through-holes are at a predetermined electric potential value.

Independent Claim 10, as amended herein, recites a semiconductor device having multiple wiring layers, with a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers. A plurality of signal lines are formed substantially in parallel to each other in different wiring layers, and to which signals having a same phase are respectively applied. A plurality of adjacent lines, each pair of which are so formed adjacent onto both sides of the signal lines, but not connected thereto in the wiring layers where the signal lines are formed. There are two intersection lines, each of which is formed in a layer under the lowermost wiring layer where the signal lines are formed, and in a layer above an uppermost wiring layer where the signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by the adjacent lines formed on the both extreme sides of said plurality of signal lines. A plurality of first entire-line-area through-holes penetrate through an insulating layer arranged between the adjacent lines and the two intersection lines, along entire areas of the adjacent lines, and thus electrically connect the adjacent lines with the two intersection lines. There are a plurality of second entire-line-area through-holes which

penetrate through an insulating layer arranged between the adjacent lines, along the entire areas of the adjacent lines, and thus electrically connects the adjacent lines with each other.

Claim 11, as amended herein, recites a semiconductor where electric potentials of the adjacent lines, the two intersection lines and the one or more first and second entire-line-area through-holes are retained at a predetermined electric potential value.

Claim 12, as amended herein, recites a semiconductor device where the electric potentials of the adjacent lines, the two intersection lines and the one or more first and second entire-line-area through-holes have the same phase as the signal lines.

Independent Claim 13, as amended herein, recites a semiconductor device having multiple wiring layers with a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers. A plurality of signal lines are formed in different wiring layers, and have signal voltages respectively applied. There are a plurality of adjacent lines each pair of which are formed either in a lowermost or uppermost wiring layer of the wiring layers where the plurality of signal lines are formed. They are respectively adjacent on both sides of a selected one of the signal lines which is formed in the same layer, but are not connected to the selected signal line. Two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of signal lines, or in a wiring layer above the uppermost wiring layer of

signal lines, and each is formed along a surface area corresponding to an area enclosed by the pair of adjacent lines formed on the both sides of the signal lines formed either in the lowermost or uppermost wiring layer of signal lines. A second intersection line is formed in a wiring layer formed between the wiring layers of signal lines, and is formed along the surface area corresponding to at least one area enclosed by the pair of adjacent lines. A plurality of first entire-line-area through-holes penetrate through insulating layers formed between the adjacent lines and the first intersection lines along the entire area of the adjacent lines, and thereby electrically connect the adjacent lines to the two first intersection lines. A plurality of second entire-line-area through-holes penetrate through insulating layers formed between the adjacent lines and the second intersection lines along the entire area of the adjacent lines, and thereby electrically connect the adjacent lines to the second intersection lines.

Claim 14, as amended herein, recites a semiconductor device where the signal voltages which are out of phase with each other are respectively applied to different signal lines.

Claim 15, as amended herein, recites a semiconductor device where the electric potentials of the first and second adjacent lines, the first and second intersection lines and the first and second entire-line-area through-holes have the same phase as the electric potential of the signal lines.

Claim 16, as amended herein, recites a semiconductor device where the signal lines formed in different wiring layers which are adjacent to each other, then intersect each other.

Independent Claim 17, as amended herein, recites a semiconductor device having a structure in which a selected signal line, to which a selected signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, whose electric potentials are set at a predetermined value.

Independent Claim 18, as amended herein, recites a semiconductor device having a structure in which a selected signal line, to which a selected signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has the same phase as the signal line is applied.

The cited art of Schreiber relates to a flexible coaxial cable capable of high frequency transmission, and is formed from a multi-layer having conducting traces embedded in a dielectric material. Selected ones of the signal traces are designated to be conducting signal lines. The signal traces may have a 360 degree signal return line formed completely around the signal line, utilizing other signal traces as part of the return line conductor. The 360 degree signal return line itself then has a 360 degree shield formed around the return line, again employing selected signal traces as part of the shield. The cable is flexible and it's structure combines to provide an even variable standing

wave ratio. Each shield 104 shares a common, substantially vertical conductor was with the neighboring shield 104, thereby joining together each adjacent coaxial structure.

Applicant respectfully submits that the cited reference does not contain the recited feature of "a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers", as set forth in independent Claim 5, as amended herein. Rather, as discussed above, Schreiber relates to a flexible coaxial cable, and contains no teaching as to integrated circuit conductor signal integrity.

Applicant further respectfully submits that the cited reference does not contain the recited feature of "a plurality of individual semiconductor devices disposed upon a semiconductor substrate having at least a plurality of insulating layers disposed between a plurality of patterned conductor wiring layers", as basically set forth in independent Claims 8, 10, 13 , as amended herein. The reasons are essentially the same as given above with reference to independent Claim 5.

Applicant further respectfully submits that the cited reference does not contain the recited feature of "a semiconductor device having a structure in which a selected one signal line of a plurality of signal lines, to which a selected signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has a same phase as a phase of said signal line is applied", as recited in independent Claims 17 and 18, as amended herein. The cited art of Schreiber

does not disclose a semiconductor nor a shield having the same phase as the signal line that it encloses.

Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claims 5, 8, 10, 13, 17 and 18. Dependent claims 6-7, 9, 11-12 and 14-16 depend from claims shown above to be patentably distinct over the cited art, and are therefore also not anticipated.

Accordingly, Applicant respectfully submits that Claims 5 - 18 are patentably distinct over the cited reference, and respectfully requests that this rejection be withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
HUTCHINS, WHEELER & DITTMAR

Date: September 12, 2000

Donald W. Muirhead
Registration No. 33,978

Patent Group
Hutchins, Wheeler & Dittmar
101 Federal Street
Boston, MA 02110